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Serial No. 10/776,101

Application of: Kim C. Hardee

Filed: February 11, 2004

Art Unit: 2819

Examiner: Not Yet Assigned Attorney Docket No. UMI-360

For: HIGH SPEED POWER-GATING TECHNIQUE FOR INTEGRATED CIRCUIT

DEVICES INCORPORATING A SLEEP MODE OF OPERATION

Confirmation No.: 2835 Customer No.: 25235

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REQUEST TO CORRECT FILING RECEIPT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

We received a Filing Receipt (copy enclosed) in the above case on May 10, 2004, which contains an error in the number of claims of the invention. The Total Number of Claims should read: 16.

Please make the indicated correction on the Filing Receipt.

Respectfully submitted,

Date:

William J. Kubida, Reg. No. 29,664

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ART UNIT

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CONFIRMATION NO. 2835

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HOGAN & HARTSON, LLP

Date Mailed: 05/10/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Kim C. Hardee, Colorado Springs, CO;

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/500,126 09/04/2003

Foreign Applications

If Required, Foreign Filing License Granted: 05/07/2004

Projected Publication Date: 03/10/2005

Non-Publication Request; No

Early Publication Request; No

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Title

High speed power-gating technique for integrated circuit devices incorporating a sleep mode of

Preliminary Class

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